# বিদ্যাসাগর বিশ্ববিদ্যালয়
# VIDYASAGAR UNIVERSITY

## Question Paper

## B.Sc. Honours Examinations 2022
**(Under CBCS Pattern)**
## Semester - IV
## Subject: ELECTRONICS
**Paper : C 9-T**
**(Digital Electronics and Verilog / VHDL)**

**Full Marks : 40**
**Time : 2 Hours**

*Candidates are required to give their answers in their own words as far as practicable.*
*The figures in the margin indicate full marks.*

1. Answer any ***four*** questions from the following : 5×4=20

(i) Implement half subtractor circuit using NAND Gates only. 5

(ii) Draw totempole configuration of a NAND gate. 5

(iii) Implement full-adcer circuit using 4×1 MUX. 5

(iv) Design a 4-bit comparator circuit. 5

(v) Differentiate between synchronous and asynchronous counter. 5

(vi) Write verilog code for XOR gate. 5

P.T.O.

2. Answer any ***two*** questions from the following : 10×2=20

(i) Design MOD-10 decade counter. 10

(ii) Describe different styles of VHDL. 10

(iii) Explain the operation of SRAM. 10

(iv) Write VHDL Code for 4-bit ripple counter. 10